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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,585	07/30/2003	Toshiyuki Kasai	116512	6186

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EXAMINER	
SHENG, TOM V	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,585	KASAI, TOSHIYUKI	
	Examiner	Art Unit	
	Tom V. Sheng	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 22 is objected to because of the following informalities: line 1, "claim 22" is obviously a typo. The Examiner believes that should be "claim 21" instead. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Okuda (US 6,380,689 B1).

As for device claims 1, 17 and associated method claims 10, 18, Okuda teaches an electronic circuit having a circuit section (light emitting circuit 10ij; fig. 15), comprising:

a first transistor (MOSFET 16; column 11, lines 18-22);

a capacitor element (capacitor 18) that stores an electrical signal supplied by said first transistor as an amount of electrical charge (capacitor 18 is charged with a

voltage signal from data line Bj during an address period; column 11, lines 37-40);

a second transistor (MOSFET 17) having a conductive state that is controlled on the basis of the amount of electrical charge stored in said capacitor element (the FET 17 is turned on or active in accordance with voltage applied to its gate from the capacitor 18; column 11, lines 47-49); and

an electronic element (EL device Eij) to which an electrical current having a current level corresponding to said conductive state is supplied (when the FET 17 is active, a current corresponding to the charge voltage in the capacitor 18 flows through the EL device Eij; column 11, lines 54-59);

wherein there are provided

a first device (**switch 56j with capacitor 57j**) that supplies a first driving voltage (**output signal from switch 56j or capacitor 57j**) to said circuit section (supplied during address period; column 11, lines 27-42); and

a second device (**switch 6i**) that supplies a second driving voltage (**either Va or -Ve**) to said circuit section (supplies Va during an address period and -Ve during an emission period). See column 11, lines 18-59.

As for claims 2, 5, 6, 11, 14, 19, 20 and 25, Okuda's sample holding circuit 55j (first device) supplies the sampled data signal (first driving voltage) from Bj during the address period (first period) and is supplied to the capacitor 18 (capacitor element). Further, Okuda's switch 6i (second device) supplies the voltage -Ve (second driving voltage) during the emission period (second period) during which the current of EL

device Eij is according to the charge or voltage (the conductive state) at capacitor 18. Further, EL device Eij is a current driven element.

As for device claims 3, 21, 22 and associated method claims 12, 26, Okuda teaches, in the rejections of claims 1 and 10, the limitations regarding the first transistor, capacitor, second transistor, electronic element, first device, first driving voltage, second device, and second driving voltage, except the limitations regarding the supplies of the first driving voltage to the second transistor and of the second driving voltage to the second transistor. This is illustrated by the supply of output signal from switch 56j and capacitor 57j to the FET 17 (via FET 16) and Va or -Ve from switch 6i to FET 17 (via EL device Eij). Alternatively, voltage -Va or Ve is supplied from switch 6i to FET 12 via EL device Eij in a variation (fig. 13; column 9, line 52 through column 10, line 5).

Please note the construct of following rejections is different from above.

As for device claims 4 and 13, Okuda teaches an electronic circuit having a circuit section (light emitting circuit 10ij; fig. 15), comprising:

a first transistor (MOSFET 16; column 11, lines 18-22);

a capacitor element (capacitor 18) that stores an electrical signal supplied by said first transistor as an amount of electrical charge (capacitor 18 is charged with a voltage signal from data line Bj during an address period; column 11, lines 37-40);

a second transistor (MOSFET 17) having a conductive state that is controlled on the basis of the amount of electrical charge stored in said capacitor element (the FET 17 is turned on or active in accordance with voltage applied to its gate from the

capacitor 18; column 11, lines 47-49);

an electronic element (EL device Eij) to which an electrical current having a current level corresponding to said conductive state is supplied (when the FET 17 is active, a current corresponding to the charge voltage in the capacitor 18 flows through the EL device Eij; column 11, lines 54-59);

wherein there are provided

a first device (**power source that supplies voltage Va**), which is connected commonly to said second transistor of each of said unit circuits (connected to all FETs 17 of row Ai via respective EL devices Eij during each address period), that supplies a first driving voltage (**voltage Va**) to each of said second transistors (supplied during address period; column 11, lines 27-42); and

a second device (**power source that supplies voltage -Ve**), which is connected commonly to said second transistor of each of said unit circuits (connected to all FETs 17 of row Ai via respective EL devices Eij during each emission period), that supplies a second driving voltage (**voltage -Ve**) to each of said second transistors. See column 11, lines 18-59.

As for method claims 7 and 15-16, Okuda teaches a method of driving an electro-optical device (light emitting circuit 10ij; fig. 15), comprising:

a first transistor (MOSFET 16; column 11, lines 18-22);

a capacitor element (capacitor 18) for storing an electrical signal supplied via said first transistor as an amount of electrical charge (capacitor 18 is charged with a voltage signal from data line Bj during an address period; column 11, lines 37-40);

a second transistor (MOSFET 17) whose conductive state is controlled on the basis of the amount of electrical charge stored in said capacitor element (the FET 17 is turned on or active in accordance with voltage applied to its gate from the capacitor 18; column 11, lines 47-49); and

an electro-optical element (EL device Eij) to which an amount of electrical current corresponding to said conductive state is supplied (when the FET 17 is active, a current corresponding to the charge voltage in the capacitor 18 flows through the EL device Eij; column 11, lines 54-59);

said method of driving an electro-optical device comprising the steps of:

supplying a first driving voltage (**Va**) to said electro-optical device in a period (the address period) in which the electrical signal (voltage signal from data line Bj, which is sampled at 55j) is supplied to a capacitor element via said first transistor (during address period, row Ai is supplied with voltage Va and FET 16 is active thus allowing sampled signal voltage to be applied to the capacitor 18; column 11, lines 27-42); and

supplying a second driving voltage (**-Ve**) lower than said first driving voltage (Va is larger than -Ve) in a period (the emission period) in which the amount of electrical current corresponding to the conductive state is supplied to said electro-optical element via said second transistor (the amount of current based on the charge at the capacitor 18 is driven at the EL device Eij via FET 17). See column 11, lines 18-59.

As for claims 8, 9, 23, 24 and 27, the EL device Eij is a current-driven EL element.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V. Sheng whose telephone number is (571) 272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Sheng
November 15, 2005

AMR A. AWAD
PRIMARY EXAMINER